

WHAT IS CLAIMED IS:

1. A bootstrap capacitor charging circuit comprising:
first and second power switching transistors arranged in a half bridge arrangement such that the first and second transistors are disposed between a high side potential and a low side potential;
5 a driver circuit for driving the first and second transistors;
a bootstrap capacitor adapted to be charged from a potential source and for providing a voltage source to power an electronic circuit;
a charging circuit providing a charging path from one of said high and low side potentials to said bootstrap capacitor;
- 10 first and second series connected switches arranged between a common node of said first and second transistors and one of said high and low side potential;
the bootstrap capacitor having a first terminal coupled to be charged by said charging circuit and a second terminal coupled to a common node between said first and second series connected switches; and
- 15 a control circuit operating in first and second modes, wherein in a first mode when said first and second power switching transistors are switching at a rate above a predetermined frequency, a first of said switches connected to said common node of said first and second power switching transistors is controlled on and said second switch is controlled off; and wherein;
20 when said first power switching transistor is on for a duration of time exceeding a preset duration, said control circuit operates in a second mode wherein said first and second switches are alternately turned on and off for first and second predefined periods of time whereby the bootstrap capacitor charges through said second switch and said charging circuit during the second predefined period of time.

2. The bootstrap capacitor charging circuit of claim 1, wherein said control circuit is operative to turn said first and second switches alternately on and off during said second mode of operation such that the first switch is on and the second switch is off for the first period of time and the first switch is off and the second switch is on for the second period of time.

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3. The bootstrap capacitor charging circuit of claim 2 wherein the first period of time is about 490 usecs the second period of time is about 10 usecs, and the preset duration is about 200 usecs.

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4. The bootstrap capacitor charging circuit of claim 1, wherein the charging circuit comprises: a regulator transistor having its main terminals connected between the potential source for charging the bootstrap capacitor and said first terminal of the bootstrap capacitor; a current source coupled between the potential source and a control terminal of the regulator transistor and further comprising a regulator element for providing a reference voltage coupled between the control terminal of the regulator transistor and said common node between said first and second switches.

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5. The bootstrap capacitor charging circuit of claim 1, wherein the charging circuit is coupled to the high side potential of said first and second switches are arranged between the common mode of the first and second transistors and said low side potential.

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6. A method for charging a bootstrap capacitor in a circuit comprising first and second power switching transistors arranged in a half bridge arrangement such that the first and second transistors are disposed between a high side potential

and a low side potential, a driver circuit for driving the first and second transistors; a bootstrap capacitor adapted to be charged from a potential source and for providing a voltage source to power an electronic circuit; a charging circuit providing a charging path from one of said high and low side potentials to said bootstrap capacitor, first
20 and second series connected switches arranged between a common node of said first and second transistors and one of said high and low side potential; the bootstrap capacitor having a first terminal coupled to be charged by said charging circuit and a second terminal coupled to a common node between said first and second series connected switches; and a control circuit for controlling the first and second switches, the method comprising:

operating said first and second switches in a first mode when said first and second power switching transistors are switching at a rate above a predetermined frequency, such that a first of said switches connected to said common node of said first and second power switching transistors is controlled on and said second switch
30 is controlled off; and

operating said first and second switches in a second mode when said first power switching transistor is on for a duration of time exceeding a preset duration, such that said first and second switches are alternately turned on and off for first and second predefined periods of time whereby the bootstrap capacitor charges through
35 said second switch and said charging circuit during the second predefined period of time.

7. The method of claim 5, wherein said step of operating said first and second switches in the second mode comprises turning said first and second switches alternately on and off such that the first switch is on and the second switch is off for the first period of time and the first switch is off and the second switch is on for the second period of time.

8. The method of claim 6 wherein the first period of time is about 490 usecs and the second period of time is about 10 usecs and the preset duration is about 200 usecs.

9. The method of claim 5, further comprising charging said bootstrap capacitor through a charging circuit comprising a voltage regulator circuit.